PATENT ABSTRACTS OF JAPAN

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(54) SAMPLING RATE CONVERTER

(57)Abstract:
PURPOSE: To markedly reduce the number of memories required for filter factors in a sampling rate converter by using a multiphase filter using an interpolation method.
CONSTITUTION: A pair of multiphase filters 20 and 30 respectively receive input digital sampling rate signals through their input terminals, but the phase selection of one multiphase filter is offset from that of the other multiphase filter by one. An interpolator 40 generates an output digital sampling rate signal by performing interpolation between the output signals of the filters 20 and 30.

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CLAIMS

[Claim(s)]

[Claim 1] The sampling rate inverter with which it is equipment which changes a digital signal into an output sampling rate from an input sampling rate, between the output signals of one pair of polyphase filters which receive the above-mentioned digital signal in an input edge with an input sampling rate, respectively, and the polyphase filter of this 1 pair is interpolated, it has a interpolation means to generate a digital signal in an output sampling rate, and only 1 offsets phase selection of one polyphase filter from the polyphase filter of another side.

[Claim 2] The sampling rate inverter of claim 1 further equipped with a means to thin out the output signal of the above-mentioned interpolation means, and to decrease the measurement size in the digital signal in an output sampling rate.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the sampling rate inverter which can reduce memory required for the conversion which has very many subphases (subphase) using a sampling rate inverter and the polyphase (polyphase) filter according to an interpolation method especially.

[0002]

[Description of the Prior Art] In much application, it may be desirable to change the digitized signal into another sampling rate from a certain sampling rate according to a format of the signal which different equipment needs. When using the polyphase filter

which calculates the data value of the signal in the time of differing from the time of sampled original, a single filter is needed to each of a desired sample secondary phase.
[0003]
[Problem(s) to be Solved by the Invention] For example, when it expresses the ratio of a desired output sampling rate and an input sampling rate with the ratio of an integer small like 33/35, in relation to one rate, the subphase of 33 (or 35) individual is between the rates of another side. As for a phase, at least each ** needs 1 sets [33] accumulated in memory, i.e., a total, of filter factors. In sampling rate conversion application which changes standard D2PAL for video into D1PAL, the number of subphases required to change correctly is 709,000 or more. Though **** is not impossible for this, it has the problem, i.e., the serious problem that the group of the filter factor of only the same number as 709,000 or more filters is needed, of using an above-mentioned transducer model.
[0004] Then, the ratio between sampling rates is expressed with the ratio of a big integer, and a sampling rate inverter using the polyphase filter which performs exact conversion, without needing the filter for Gentlemen phases is desired.
[0005] Therefore, the purpose of this invention is in offer of the sampling rate inverter which reduced memory required for a filter factor sharply using the polyphase filter by the interpolation method.
[0006]
[Means for Solving the Problem] According to this invention, it is combined with the common source of an input signal, and only the subphase of one piece from the polyphase filter of another side is offset, and one polyphase filter drives the input edge of one pair of polyphase filters. The output signal of these polyphases filter turns into an input signal of a linear interpolation machine. the time of carrying out the multiplication of the resolution of this linear interpolation machine with the resolution of a polyphase filter -- the resolution of this whole system -- it is enough for extent suitable for a demand.
[0007] Other purposes, advantages, and new descriptions of this invention will become clearer than explanation of the following which referred to the attached drawing.
[0008]
[Example] Drawing 1 shows the sampling rate inverter 10 by this invention. Each of the two same polyphase filters 20 and 30 of a design is N phase. The input data sampled with the 1st sampling rate is inputted into both polyphase filters 20 and 30. The coarse control phase command from a controller (not shown) is inputted into the phase selection terminal of one polyphase filter 30. The same coarse control phase command to which the increment only of 1 was carried out with the adder 25 is inputted into the phase selection terminal of the polyphase filter 20 of another side. The output signal from the polyphase filters 20 and 30 is inputted into the input edges A and B of the linear interpolation machine 40, respectively. The fine control phase

command from a controller is inputted into the control terminal Z of an interpolator 40. The output-data signal of the 2nd sampling rate is generated in the output terminal C of an interpolator 40. This output-data signal becomes like a degree type.
C=Z*A+(1-Z) *B -- still in addition, A, B, C, and Z express the signal of each terminal, and * means multiplication. Moreover, Z has M step between 0 and 1. At least that of the polyphase filters 20 and 30 of the resolution as a result of an output-data signal is the product of a source resultant pulse number N and number-of-steps M of a fine control command signal. That is, this resolution is N*M. The linear interpolation machine 40 is between the phases of the polyphase filters 20 and 30, and generates a subphase at equal intervals.

[0009] An example of the decoder 50 using the sampling rate inverter by this invention is shown in drawing 2 . The digital composite video signal of a D2PAL format is changed into the digital composite video signal of a D1PAL format using this decoder 50. D2 input signal of a 177M (megger) bit sampling rate is inputted into the circuit 52 non-serializing (serial parallel conversion), and it changes into the flow of the parallel data of the 10-bit data word of a 17.7MHz clock rate. The flow of this parallel data is inputted into a decoder circuit 54, and Y component data flow for luminance (brightness) and C component (interleave is carried out) data flow for chrominances (color) are generated. These [Y] and C data flow are inputted into the rate transducer circuit 56, and it changes into D1 data rate of 27MHz by this invention. This D1 parallel data is inputted into the serialization (parallel serial conversion) circuit 58, and it changes into the standard serial data for EBU3267E of a 270 M bit sampling rate.

[0010] The detail of the rate converter circuit 56 is shown in drawing 3 . In addition, in this drawing, the illustrated frequency shows the conversion to D1PAL from D2PAL. Y and C data signal which were decoded -- respectively -- the anti alias filters 60 and 62 -- minding -- the sampling rate inverters 10 and 10 -- a clock is carried out to 'the inner polyphase filters 20 and 30 and 20', 30' (inputted for every clock). Although a sequence and a controller 65 supply a filter factor value to each polyphase filter, this multiplier is also performing the operation of the adder 25 shown in drawing 1 while it is equivalent to a multiplier required for the present phase and the following phase. (Although the signal line is connected in addition common to each circuit from the sequence and the controller 65 by drawing 3 , please care about the point that a signal is supplied for every circuit, in fact.) The output signal of the polyphase filters 20 and 30, 20', and 30' is inputted into the linear interpolation machine 40 and 40'. The output signal of these interpolators 40 and 40' is inputted into the FIFO (first in first out) buffers (DESHIMETA FIFO) 64 and 66, respectively. These FIFO buffers drop the 3rd sample in the 4th [every] effectively (thinning out), and generate a desired output frequency. In this example, in an output sampling rate, i.e., 13.5MHz, FIFO buffers 64 and 66 sample an interpolator 40 and the juxtaposition output from 40', and thin out 1135 samples per line about the combination of 864 chroma (chrominance)

samples per line, and a luminance sample. The format multiplexer (MUX) circuit 68 generates a desired output signal combining output Y data and output C data flow.
[0011] The detail of DESHIMETA FIFO 64 for Y data flow is shown in drawing 4 . Since the offset for every frame of a subcarrier frequency is 1Hz in PAL and there is no PAL sample on an orthogonal cross grid, there is no multiple of a rational common sampling rate. Therefore, DESHIMETA FIFO 64 needs many output phases. In order to acquire a desired precision, two FIR (finite impulse response) filters 70Y and 72Y are used. Each of these filters has a different multiplier value from ten taps. The output signal of the FIR filters 71Y and 72Y is inputted into linear interpolation machine 74Y of 64 steps. A dither is applied to interpolator 74Y, and this interpolator generates the output signal of bits fewer than the output signal originally generated, and may improve quantization straight-line control. This output is calculated at 4fsc input rate (fsc is a subcarrier frequency), one sample is dropped for every 3rd piece or 4th clock (thinning out), and an average output sampling rate is generated. The output signal of interpolator 74Y is inputted into are recording buffer 76Y which is FIFO. This are recording buffer is the output sampling rate fo. Data output is read. Time amount amendment for a suitable output sampling rate is performed using this FIFO76.
[0012] As similarly shown in drawing 5 , DESHIMETA 66 for chroma data flow contains the FIR filters 70C and 72C, linear interpolation machine 74C, and output FIFO76C, and these operate like DESHIMETA 64 for luminance data flow. The sequence equalization circuit 78 is inserted between interpolator 74C and FIFO-buffer 76C. This sequence equalization circuit 78 decides which chroma value between U and V component to throw away according to an input bias signal. This condition is shown in the lower right of drawing 5 .
[0013]
[Effect of the Invention] According to the sampling rate inverter of this invention, like ****, memory required for conversion can be reduced using the polyphase filter by the interpolation method to the conversion during the digital data format which has very many subphases.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the rough configuration of the sampling rate inverter by this invention.
[Drawing 2] It is the block diagram of a decoder using the sampling rate inverter by this invention.
[Drawing 3] It is the block diagram of the sampling rate inverter by this invention for

the decoders of drawing 2 .

[Drawing 4] It is the block diagram of the luminance sampling rate inverter by this invention for the decoders of drawing 2 .

[Drawing 5] It is the block diagram of the chroma sampling rate inverter by this invention for the decoders of drawing 2 .

20 30 Polyphase filter

40 Interpolation Means